EXPEDITED PROCEDURE - EXAMINING GROUP 2815

S/N 08/903,453 **PATENT**

#38 Response

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: George C. Eckert II	
Serial No.:	08/903,453	Group Art Unit: 2815	
Filed:	July 29, 1997	Docket: 303.378US1	
Title:	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS		

J Mueller 10/16/02

RESPONSE UNDER 37 C.F.R. § 1.116

Box RCE
Commissioner for Patents
Washington, D.C. 20231

In response to the final Office Action dated 21 June 2002, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are pending in the application, and are rejected. None of the claims have been amended.

Double Patenting Rejection

Claims 2 and 3 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims in co-pending Application No. 08/902,843. The applicant will address this rejection when the claims are otherwise indicated as allowable.

Rejection of Claims under §103

Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were rejected under 35 USC § 103(a) as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata), in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). The applicant respectfully traverses.

Claim 24 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 a heterojunction (HJ) diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, Column 3. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 24.

Sugita shows a floating gate transistor with a source and a drain in a substrate, and a polysilicon floating gate separated from the substrate by an insulator.

However, there is no suggestion or motivation to combine Sakata and Sugita.

The applicant has submitted pages from two textbooks, Sze and Streetman, in an IDS filed with this response. The applicant incorporates herein the remarks made in the response filed on 21 March 2002. In furtherance of the arguments made therein, the applicant respectfully submits that the selections from Sze and Streetman demonstrate that a heterojunction structure is substantially different from the floating gate transistor shown in Sugita and in other sources mentioned in the final Office Action.

Sze defines a heterojunction as "a junction formed between two dissimilar semiconductors." Sze, page 122. Heterojunctions are used in bipolar transistors and optoelectronic devices such as lasers, light-emitter diodes, photodetectors, and solar cells. Sze, page 122. Sakata is clearly referring to this class of semiconductor devices when he states that "[a]lthough the application of the heterojunction (HJ) composed of hydrogenated .... has been limited to optoelectronic devices." Sakata, page 688, column 1.

Sze shows several examples of heterojunction structures. Figures 19-21 on pages 701-703 of Sze show LEDs. Figure 26 on page 708 of Sze shows a laser as a two-terminal device, with terminals on the top and bottom of a stack and current I flowing orthogonally through the layers. Figures 17 and 18 on pages 764 and 765 show photodiodes. Figure 17 shows contacts on the top and bottom of the stack and Figure 18 shows the circuit of the photodiode coupled between contacts on the top and bottom of the stack.

Streetman also shows examples of heterojunction structures. Figure 6-16 shows a schematic of a p-i-n photodiode on page 218 of Streetman with a circuit coupled between top and

bottom contacts. Multilayer heterojunction structures are shown in Figure 6-17 on page 219 of Streetman. Heterojunction laser structures are shown on pages 392-393 of Streetman.

None of these heterojunction structures show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 24.

The final Office Action states that the motivation for combining Sakata and Sugita is that "the source, drain, and channel regions allow individual floating gate devices to be formed in an array....[t]he use of the source/drain/channel regions for such programming is well known in the art." Final Office Action, page 5. This theory of obviousness is contradicted by the evidence in Sze and Streetman that heterojunction structures are substantially different from floating gate transistors, and have a different principle of operation. The diode structure of Sakata is so fundamentally different from the floating gate transistor of Sugita that one skilled in the art would not have been motivated to add a source region and a drain region to a substrate of Sakata. An addition of elements from Sugita to the HJ diode structure of Sakata would change the principle of operation of Sakata, and therefore the teachings of Sakata and Sugita are not sufficient to render claim 24 *prima facie* obvious.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 24 has **not** been established in the final Office Action, and that claim 24 is in condition for allowance. Claims 25-28 and 44 are dependent on claim 24, and recite further limitations with respect to claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 25-28 and 44 has **not** been established in the final Office Action, and that claims 25-28 and 44 are in condition for allowance.

Claims 2, 3, 41-43, 45-48, 50-52, and 65-68 recite elements similar to those recited in claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 41-43, 45-48, 50-52, and 65-68 has **not** been established in the final Office Action, and that claims 2, 3, 41-43, 45-48, 50-52, and 65-68 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 23 September 2002 By _____

Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 23rd day of September, 2002.

Name Amy Moriarty

Signature _____

RCE/2815

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Application Number	08/903,453
Filing Date	July 29, 1997
First Named Inventor	Leonard Forbes et al.
Group Art Unit	2815
Examiner Name	George C. Eckert II
Attorney Docket Number	303.378US1

#36
Req for RCE
J McMillan 10/16/02

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application entitled CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS .

Submission required under 37 C.F.R. § 1.114

1. _ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on __
2. _ Consider the arguments in the Appeal Brief or Reply Brief previously filed on __
3. X A Response Under 37 CFR § 1.116 (4 pages) is enclosed.
4. _ A new power of attorney (_ pages) is enclosed.
5. X An Information Disclosure Statement is enclosed (1 page)
   a. 1 Form(s) 1449
   b. 17 Copies of IDS Citations
6. X A check in the amount of $740.00 is attached to pay the RCE filing fee required under C.F.R. § 1.17(e).
7. X **The Commissioner is hereby authorized to credit overpayments or charge any fees set forth in 37 C.F.R. §§ 1.16 through 1.18 to Deposit Account No. 19-0743.**
8. _ A petition for extension of time in the prior application (_ pages) is enclosed along with a check in the amount of $ to pay the extension fee.
9. _ Other:

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By: _____
Atty: Robert E. Mates
Reg. No. 35,271

Customer Number 21186

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Name Amy Moriarty

Signature _____